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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/481,388	01/12/2000	Jeffrey Dwork	52352-310	5577

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EXAMINER
PATEL, NIKETA I

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/481,388	DWORK, JEFFREY	
	Examiner	Art Unit	
	Niketa I Patel	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *6 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Objections

2. Claim 6 is objected to because of the following informalities: the word "***multiplexer***" is misspelled in line 2 on page 10. Appropriate correction is required.

3. Claim 16 is objected to because of the following informalities: the word "***path***" is misspelled in line 1 on page 12. Line 1 recites "*where in the **pass** for*", it should recite "*where in the **path** for*". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaczmarczyk et al. (U.S. Patent Number 5,625,796) and further in view of Singh et al. (U.S. Patent Number 6,425,093)

6. Referring to claim 1, Kaczmarczyk teaches a host interface (see figure 6 – element 1) for providing address, data and control signals from a host (see figure 6 – elements A, C, D and

column 7 – lines 46-59), a storage element for holding data accessible via the host interface (see figure 6 – element 9), and alternate access circuitry for providing access to the storage element so as to access the data as a first data element in a first register (see figure 6 – element 43, 7, 9, 4 and 1), and as a second data element in a second register (see figure 6 – elements 2, 5 43, 7 and 9.)

Kaczmarczyk fails to explicitly teach a fist type of software and a second type of software that are stored in the storage element. However, Singh teaches to store a first and a second type of software in a storage element (see figure 6 – elements 302, 306 and column 8 – lines 33-61.)

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the data processing system of Kaczmarczyk to have more then one type of software so that it would allow the user of the processing system have a music software and word processing software which would allow a user to listen to music while typing a document using the word processing software. It is for this reason that one of ordinary skill in the art would have been motivated to substitute Kaczmarczyk's storage element with a storage element comprising a plurality of software storage capability to allow a user to perform multiple tasks at the same time.

7. Referring to claim 2, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches an alternate access circuitry is configured to perform writing data into the storage element in response to a fist address signal supplied from the host interface to access the first register, when the system operates with the first type of software (see column 4 – lines 61-67.)

8. Referring to claim 3, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches an alternate access circuitry is configured to perform writing data into the storage element in response to a second address signal supplied from the host interface to access the second register, when the system operates with the second type of software (see column 4 – lines 61-67.)

9. Referring to claim 4, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches an alternate access circuitry is configured to perform reading data from the storage element in response to a first address signal supplied from the host interface to access the first register, when the system operates with the first type of software (see column 5 – lines 11-21.)

10. Referring to claim 5, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches an alternate access circuitry is configured to perform reading data from the storage element in response to a second address signal supplied from the host interface to access the second register, when the system operates with the second type of software (see column 5 – lines 22-35.)

11. Referring to claim 6, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches an alternate access circuitry (see figure 4 – element 3) comprises a writing multiplexer (see figure 4 – element 32) having a first input for supplying the first data element to the storage element when the system operates with the first type of software, and a second input for supplying the second data element to the storage element when the system operates with the second type of software (see column 5 – lines 60-67 and column 6 – lines 1-7, 37-53.)

12. Referring to claim 7, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a writing multiplexer is controlled by a first select signal to pass the first data element to the storage element when the first select signal is asserted (see column 4 – lines 15-37.)

13. Referring to claim 8, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a writing multiplexer is controlled by a second select signal to pass the second data element to the storage element when the second select signal is asserted (see column 4 – lines 15-37.)

14. Referring to claim 9, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a first select signal is asserted in response to a fist address signal supplied from the host interface to access the first register (see column 4 – lines 15-37.)

15. Referring to claim 10, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a second select signal is asserted in response to a second address signal supplied from the host interface to access the second register (see column 4 – lines 15-37.)

16. Referring to claim 11, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches an alternate access circuitry (see figure 4 – element 3) comprises a first reading gate (see figure 4 – element 32) coupled to the storage element for outputting the first data element when the system operates with the first type of software, and a second reading gate coupled to the storage element for outputting the second data

element when the system operates with the second type of software (see column 5 – lines 60-67 and column 6 – lines 1-7, 37-53.)

17. Referring to claim 12, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a first reading gate is configured to output the first data element in response to a first address signal supplied from the host interface to access the first register (see column 4 – lines 15-37.)

18. Referring to claim 13, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a second reading gate is configured to output the second data element in response to a second address signal supplied from the host interface to access the second register (see column 4 – lines 15-37.)

19. Referring to claim 14, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a host interface (see figure 6 – element 1) for supplying address, data and control signals from a host (see figure 6 – elements A, C, D and column 7 – lines 46-59), a storage element for holding a data element accessible via the host interface (see figure 6 – element 9), and alternate access circuitry coupled to the storage element for providing multiple paths for accessing the data element (see figure 6 – element 43, 7, 9, 4, 5, 2 and 1.)

20. Referring to claim 15, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches an alternate access circuitry is configured to select a path for accessing the data element depending on a type of software used to operate the network interface (see column 4 – lines 15-37.)

21. Referring to claim 16, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches a path for accessing the data element is allocated in response to an address signal supplied from the network interface to access a predetermined register, when a selected type of software is used to operate the network interface (see column 4 – lines 15-37 and column 7 – lines 46-59.)

22. Referring to claim 17, the apparatus of Kaczmarczyk as modified by the apparatus of Singh et al. as applied to claim 1 above teaches that a selected type of software requires the data element to be held in the predetermined register (see column 5 – lines 22-35.)

23. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (U.S. Patent Number 6,425,093) and further in view of Kaczmarczyk et al. (U.S. Patent Number 5,625,796)

24. Referring to claim 18, Singh teaches a method of providing access to a storage element for holding a data element, comprising the steps of: accessing the storage element via a first access path when a first type of software is used to operate the data processing system, and accessing the storage element via a second access path when a second type of software is used to operate the data processing system (see column 8 – lines 33-61 and column 3 – lines 8-21, 34-36, 42-50.)

25. Referring to claim 19, Singh teaches a first type of software to hold data elements (see figure 6 – element 302.) Singh fails to explicitly teach a first access path allocated in response to a first address signal identifying a first register. However, Kaczmarczyk teaches a first access

path allocated in response to a first address signal identifying a first register (see figure 4 – elements 2, 5, 32, 7 and 9.)

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the data processing system of Singh to have a first access path to allow an access to the stored data so that the application can be utilized. It is for this reason that one of ordinary skill in the art would have been motivated to substitute Singh's data processing element with a one that has access path so that the user can utilize the stored data.

26. Referring to claim 20, Singh teaches a second type of software to hold the data element (see figure 6 – element 306.) Singh fails to explicitly teach a second access path is allocated in response to a second address signal identifying a second register. However, Kaczmarczyk teach a second access path is allocated in response to a second address signal identifying a second register (see figure 4 – elements 1, 4, 32, 7 and 9.)

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the data processing system of Singh to have a second access path to allow an access to the stored data so that the application can be utilized. It is for this reason that one of ordinary skill in the art would have been motivated to substitute Singh's data processing element with a one that has access path so that the user can utilize the stored data.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made record of to further show the state of the art as it pertains to data processing systems with plurality of software.

Ohara U.S. Patent Number 6,286,070

Hughes U.S. Patent Number 5,784,582

Hill et al. U.S. Patent Number 5,987,605

Nguyen et al. U.S. Patent Number 5,887,163

Park U.S. Patent Number 6,079,016

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The examiner can normally be reached on M-F 9:00am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746 7239 for regular communications and (703) 746 7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

NP
December 5, 2002

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100